

**IN THE SPECIFICATION:**

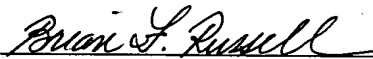
Please add at page 1, line 1:

This national stage application claims the benefit of:

U.S. Provisional Application No. 60/184,192, filed on 22 February 2000, and  
entitled "*Method and Apparatus for Wafer and Device Level Testing for an RSL Logic  
Device,*" and

U.S. Provisional Application No. 60/234,647, filed on 22 September 2000, and  
entitled "*Memory Tester Architecture.*"

Respectfully submitted,



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